Preliminary General Specifications for a Transverse Feedback System in SIS100

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Overview

This reports presents the main features of the Transverse Feedback System (TFS) which should be designed for the SIS100 synchrotron. The general parameters for the SIS100 synchrotron and the basic specifications for the TFS in SIS100 are summarized in the Tables at the end of the report.

The present status of the Transverse Feedback System (TFS) implies the usage of the standard BPM pick-ups of the SIS100 beam diagnostics. This means that the input signal of the TFS would be the digitalized and processed signal from the ADC and FPGA in the BPM frames located in the accelerator tunnel. One of the important decisions for the TFS design is whether the standard SIS100 BPMs should be employed, or dedicated pick-ups should be required. Assuming the usage of the standard BPMs the following TFS components should be considered:

- Pick-ups and the related amplifiers
- ADC and the FPGA processing in the BPM frame
- Automatic delays for individual pick-up signals
- FPGA processing in the TFS frame
- Automatic delays for the main signal (multiple set-ups)
- BOSS System
- Notch Filter
- Low-Pass Filter
- BTF System
- Switch
- DAC
- Kicker Signal Amplifier
- TFS Kicker

Operation Type

Two main tasks should perform the TFS at SIS100, compensation of the transverse injection errors with a minimum emittance blow-up, and the suppression of the coherent instabilities, mainly the high-order (e.g. $k = 4$) head-tail modes in the U^{28+} bunches at the injection energy. The basic $k = 0$ mode is located around 5 MHz in the spectrum, for damping of the most dangerous resistive-wall driven instabilities the lower frequencies are most important.

High-frequency instabilities, for example those due to electron clouds (from the experience with the long bunches at SNS, Oak Ridge: 20–100 MHz) are not the target of the TFS at SIS100, according to the present status.

A transverse feedback systems can work in the "bunch-by-bunch" mode which implies sampling of the total bunch offset and applying the processed value to kick the complete bunch by one deflection. In the "multi-sampling per bunch" mode several transverse offsets are measured and, correspondingly, several different kicks are applied along the bunch length. Since the odd head-tail modes $k = 1, 3, ...$ have a zero total offset for the chromaticity $\xi = 0$, a "bunch-by-bunch" TFS can be inefficient at small chromaticities. In the "bunch-by-bunch" mode the TFS sampling frequency must be attached to the revolution frequency and to the harmonic number. In the "multi-sampling" mode a fixed TFS sampling frequency (in Hz) can be possible, which would mean a varying number of samples during the magnetic ramp or for bunches with different lengths.

In the case of SIS100, the bunches are long with regard to the betatron phase advance. For example for the nominal U^{28+} bunches at the injection energy, the betatron phase shift over the bunch length is $\chi_b = Q_0 \xi L_b/(R\eta) \approx 12$ which means that even the basic $k = 0$ mode has nearly two wiggles along the bunch. Thus, in the "bunch-by-bunch" mode the efficiency of injection errors compensation, where the low-order head-tail modes have usually large contributions, is expected to be low. Due to this factor, and keeping in mind the high-order head-tail instabilities to be damped by the TFS, also for small chromaticities, it is suggested to choose the "multi-sampling" mode for the TFS in SIS100.

Sampling Frequency and Bandwidth

Usually the sampling frequency is a multiple of the revolution frequency and hence changes during the magnetic ramp. This has many advantages for the technical implementations, for example the notch filter. This also provides the identical clock for all the TFS components, and allows to keep the number of the sampling points per rf bucket constant during the cycle.

Assuming the usage of the SIS100 standard BPM system, the sampling rate is fixed to 8 ns, and the multiple of this rate should be used in the TFS. Summation over several samples can be done in the FPGA module of the BPM frame. Assuming that four points per wave is enough to damp a transverse mode, the sampling rate of 24 ns, i.e. the sum over three BPM samples, should provide damping up to 10 MHz.

The sampling frequency can be limited by the available data transfer rate. The BPM pick-ups at SIS100 should be built in frames, where the output communication module provides 4 GBit/s. Assuming a 24 ns sampling rate, the four 12 Bit BPM plate signals and three 8 Bit technical signals result in 3.2 GBit/s.

The aspects of a fixed sampling frequency should be further investigated, the upper border of the bandwidth can be defined as 10 MHz.

The lower limit for the bandwidth corresponds to the lowest betatron line, for the horizontal tune $Q_0 = 18.84$ during the heavy-ion operation at the injection energy it is 25 kHz.

Serial–parallel connections for the data communications and different clocks in devices produce jitter, which limits the available band width. For the bandwidth 10 MHz, and assuming 10° phase tolerance, the maximum allowable jitter is 2.8 ns. For the bandwidth 20 MHz it is 1.4 ns.

Pick-Ups

The following requirements and questions are the issues with regard to the pick-ups.

The bandwidth of the pick-up assembly and the BPM amplifier should meet the general TFS requirements: the low operation border is 25 kHz, the upper limit is 10 MHz. The amplifier gain should be adjustable cycle-by-cycle.

In order to provide a safe dynamic range the ADC should digitalized the Δ-signals at least with 16 Bit. Additional amplifiers before ADC should be foreseen for the pick-up signals in the reachable area to guarantee an opportunity to adjust the dynamic range for the given operation.

The present concept for the TFS system in SIS100 is a multiple pick-up set-up which should compensate the optics errors and is a PhD project of M. Alhumaidi at TU Darmstadt. The important decision for the next future concerns the number of pick-ups employed for the TFS.

The option of the operation with a single pick-up must be foreseen. In probable cases of technical problems of the individual pick-ups, or especially problems in the TFS connected with the combining of the different pick-ups signals, the operation with a single pick-up can still provide all the TFS functions. This can be implemented with, for example, a Hilbert filter in a two-turn mode.

Basing on the chosen number of pick-ups, specific BPMs from the available SIS100 BPM system should be appointed. In TFS systems with two pick-ups the optimal efficiency is provided for a quarter-wavelength (or 90°) of the betatron phase between the pick-ups. Another factor for the BPM appointment is the resulting cable lengths and the related delays.

Automatic delays

The time for the signal travel from a pick-up to the kicker must be equal to the time of the particle flight in the accelerator,

$$T_{\mathrm{PU}} + T_{\mathrm{processing}} + T_{\mathrm{cables}} + T_{\mathrm{delay}} = T_{\mathrm{flight}} + nT_{\mathrm{turn}} \ ,$$

here T_{PU} is the individual adjustable automatic delay for each pick-up. The fixed time $T_{\mathrm{processing}}$ includes the time of the signal processing in the ADC, FPGA of the BPM frame and FPGA of the TFS frame, and in the DAC. The signal travel time in cables T_{cables} is also individual for every pick-ups and is fixed. The number of turns n between the beam measurement and the TFS kick should be ideally $n = 0$ (next-turn kick) but can be chosen larger due to a longer signal travel in the TFS hardware. The efficiency of a feedback system with higher n should be investigated. The automatic adjustable delays T_{delay} depend on the revolution frequency and on the chosen n. All the delays T_{PU} and T_{delay} should be automatically adjusted along the magnetic ramp.

Preliminary estimations: ADC and DAC delays are $0.5\,\mu$s each, FPGA delay is $1.5\,\mu$s, the total cable delay is $1\,\mu$s, provide a delay of approximately $3.5\,\mu$s. Comparing with the SIS100 turn times we may conclude that a next-turn operation should be possible.

Main Signal Processing

An important task for the signal processing in the FPGA of the TFS frame (or in the central FPGA for the system with a single circuit) is the combining the different pick-up signals for the multiple pick-up mode. or the Hilbert filter for the single pick-up mode.

An important choice concerns the method of the feedback signal implementation. The BPM signal is the dipole moment, which is proportional to the local line density (or intensity) and to the local offset $\Delta V = \Delta x \times \lambda$. Three different methods for the TFS signal implementation are possible:

1. The pick-up signal normalized to the local line density,

$$u_\mathrm{v} = \frac{V_1 - V_2}{V_1 + V_2 + H_1 + H_2} \ ,$$

   here for the vertical signal. The TFS damping rate does not depend on the beam intensity with this method .

2. The pick-up signal is not normalized,

$$u_\mathrm{v} = V_1 - V_2 \ .$$

   This method corresponds to a constant equivalent damping impedance. The damping rate is stronger for higher intensities with a linear dependence, in the same way as the instability growth rate.

3. The kick power is constant and depend only on the sign of the beam signal ΔV. This so-called "bang-bang" method provides a non-exponential damping.

The first method (with the normalization) has a drawback in the multi-sample operation for the bunch tails where the normalization will increase the noise and heat the beam. The second method is usually chosen for the wide bandwidth feedback systems. The optimal method for the TFS in SIS100 should be chosen taking into account different TFS operation modes for different SIS100 ion operations. The amplifier saturation can bring the system into the bang-bang mode for certain cycle periods. The implementation in the FPGA of the TFS frame should provide flexibility to change the signal method in the cycle-by-cycle basis.

Additionally, the FPGA of the TFS frame should include the notch filter, and, optionally, the BOSS system and the low-pass filter.

BOSS, Notch Filter

Special measures are necessary to cope with the closed-orbit errors at the positions of the pick-ups. These errors can cause a saturation of the TFS kicker amplifier for the chosen gain. Second, the TFS can affect the closed-orbit in SIS100 which should be avoided. Third, the spectral components due to the bunch structure in the amplified signal can have a heating effect on the transverse beam oscillations.

Two system components can be used to deal with the closed-orbit errors.

The first is a Beam Offset Signal Suppression (BOSS), which subtracts the average beam position in the pick-up signals before the signal processing. This can be done by the control of the individual pick-up plate amplifiers, or probably by the digital signal processing prior to the main FPGA processing in the TFS frame. The response time should be checked and compared with the expected time scale of the closed-orbit changes.

The second component is a notch filter which suppresses the harmonics of the revolution frequency f_0. As an example, the notch filter at the SNS damping system shows an attenuation of 50 dB. Another requirement concerns the notch steepness: at the distance of $0.1f_0$ from any f_0–harmonics the attenuation and the phase rotation should be small enough.

Low-Pass Filter

A low-pass filter is necessary to reduce the system noise and thus to increase the efficiency. It should be adjustable in the cycle-by-cycle basis. Generally, a low-pass filter should be around the upper limit of the frequency function, 10 MHz, the required attenuation is usually around 50 dB. The exact frequency of the filter should be investigated, in view of the TFS efficiency for different accelerator operation modes.

BTF System

A Beam Transfer Function (BTF) system as a part of the TFS is necessary for the function tests and for the BTF measurements, which is an essential beam diagnostics. The BTF calculations can be implemented in the FPGA of the TFS frame. Alternatively, only the BTF signal inputs/outputs can be foreseen for the external implementations.

Kicker, Gain, Switch

The kicker gain should be carefully chosen especially for the compensation of the transverse injection errors. The TFS should provide an amplitude decay which is faster than the filamentation and the nonlinearities damping. At the same time, the transverse emittance blow-up should be minimized. Further studies, including particle tracking simulations, are necessary in order to define the optimum gain. The kicker amplifier should correspond to the general bandwidth requirements.

An alternative with two kickers, one for the horizontal plane, another one for the vertical plane, should be considered. This would improve the coupling efficiency because the kickers can be positioned in the optimal beta function locations, the horizontal kicker in the optimum beta function position in the lattice, and the vertical kicker correspondingly. This alternative would also allow for an optimized design of the kicker hardware, in order to obtain a better efficiency in the horizontal/vertical plane.

The kicker gain should be adjustable, with a possibility of the varying gain along the accelerator cycle. This is due to different kick power requirements for the compensation of the transverse injection errors, and for the instability suppression during the acceleration. It should be possible to change the gain scenario cycle-by-cycle depending on the accelerator operation.

A fast switch should be foreseen in order to put the TFS inactive for desired time intervals during the accelerator cycle.

Table 1: General parameters of the SIS100 synchrotron

Ring Radius R	172.46 m
p^+ injection γ / top γ / γ_t	5.26 / 31.9 / 45.505
U^{28+} injection γ / top γ / γ_t	1.21 / 2.6 / 15.59
p^+ lattice Q_{0x}/Q_{0y}	21.78 / 17.4
U^{28+} lattice Q_{0x}/Q_{0y}	18.84 / 18.73
Revolution Frequency f_0	U^{28+}: 156.6 kHz–255.4 kHz p^+: 271.6 kHz–276.5 kHz
Turn Time	U^{28+}: 6.4μs–3.9μs p^+: 3.7μs–3.6μs

Table 2: Basic parameters for the TFS in SIS100

System Operation	wide-bandwidth feedback multi-sampling mode
Bandwidth: low border (-1 dB)	25 kHz
Bandwidth: upper border (-1 dB)	10 MHz
Total Signal Jitter	max. 2.8 ns
ADC	16 Bit for the Δ–Signal 100 MHz

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